MANUFACTURE OF SILICON SUBSTRATE FOR SEMICONDUCTOR DEVICE

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Equivalents:	

Abstract

PURPOSE:To enable distribution of internal defect to be uniform when manufacturing a device by cooling it to a room temperature at a specified rate rapidly after heating it to a required temperature by irradiation with light.

CONSTITUTION:Light of xenon lamp or halogen lamp is directed to a silicon substrate above 1200 deg.C and then it is cooled down to a room temperature at 2.2 deg.C/sec or more rapidly. With this preliminary treating, cores with a non- uniform internal defect introduced on growth of a silicon single crystal are nearly extinguished and internal defects occur uniformly on the silicon substrate during device production process by a new and highly concentrated atomic empty hole distributed uniformly. Then, concentration of oxygen between grids is reduced at a device active area near the surface, thus resulting in an area without any internal defect.

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Specifications

1. Title of the Invention: Manufacturing Method for Silicon Wafer for Semiconductor Device Use

2. Scope of the Patent Claims

(1) A method for production of a silicon wafer for semiconductor device use; wherein the method comprises the step, after irradiation of the semiconductor silicon wafer with light from a xenon or halogen lamp, of rapidly cooling to room temperature at a rate of 2.2°C/second or more.

3. Detailed Explanation of the Invention

Industrial Field of Use

This invention relates to a method for manufacture of a silicon wafer used for semiconductor devices.

Earlier Technology

Most silicon wafers used for semiconductor devices are grown by pulling (CZ method).

Silicon single crystal grown by this CZ method normally contains 10^{18} cm^{-3} added oxygen component. When such silicon single crystal is used without further treatment in device production processes, the supersaturated added oxygen component precipitates during processing. Moreover, secondary dislocations, stacking faults, etc. (hereinafter these precipitates, dislocations, stacking faults, etc. are simply referred to as internal defects) are generated due to warping caused by volumetric expansion of these oxygen precipitates.

These internal defects greatly affect characteristics of semiconductor devices. When a defect exists in the device active layer, leakage current increases so as to cause oxidation layer breakdown voltage failure, etc. However, these become a source of gettering for contaminant impurities introduced during device manufacturing processes, thereby improving device characteristics. Therefore control of the generation of internal defects is important.

Silicon single crystal grown by the CZ method is processed into wafers and is conventionally used as silicon wafer for device production steps without further processing.

Problems to be Solved by the Invention

When silicon single crystal grown by the CZ method is processed into wafers and is used as a silicon wafer for device production steps without further processing as described above, internal defects are generated with a distribution corresponding to growth nuclei introduced according to thermal history undergone during silicon single crystal growth. As a result, internal defects are generated non-uniformly within the wafer, and device characteristics are made worse.

The object of the present invention is to provide a method to solve the above mentioned problem points.

Means to Solve the Problems

This invention is a method for production of a silicon wafer for semiconductor device use; wherein the method comprises the step, after irradiation of the semiconductor silicon wafer with light from a xenon or halogen lamp, of rapidly cooling to room temperature at a rate of 2.2°C/second or more.

This invention, by carrying out the above mentioned heat treatment prior to use of the silicon wafer for device manufacturing processes, imparts uniform formation of internal defects within the silicon wafer both within the silicon wafer and across the silicon wafer surface.

Due to the above mentioned heat treatment, interstitial oxygen of the silicon wafer diffuses outward, and interstitial oxygen concentration decreases in the vicinity of the surface. Moreover, growth or disappearance of internal defect growth nuclei introduced during silicon single crystal growth is determined according to a temperature-dependent critical size. Therefore internal defect growth nuclei of this silicon wafer mostly shrink and disappear. In addition, the concentration of silicon interstitials decreases due to diffusion, and atomic vacancy concentration of this silicon wafer increases.

If the heating temperature during the above mentioned heat treatment is less than 1200°C, a longer time period is required for outward diffusion of interstitial oxygen and disappearance of internal defect growth nuclei.

Although rapid cooling after heating is carried out down to room temperature by a means such as contacting with exterior air, the introduction of new internal defect growth nuclei is controlled during cooling by this rapid cooling treatment. Furthermore, a uniform distribution of atomic vacancies at a high concentration are frozen into the interior of this silicon wafer.

Moreover, use of a xenon lamp or a halogen lamp for heating makes possible heating to a high temperature in comparison to use of a diffusion furnace. A xenon lamp or halogen lamp is also used due to high heating rate which is capable of shrinking the heating time period. Heating by this type of lamp is preferably carried out in an inert gas atmosphere comprising high purity nitrogen gas, etc. Use of such an atmosphere is preferred for increasing outward diffusion of interstitial oxygen and lessening of atmospheric-derived contamination during heating.

Furthermore, generation density of internal defects can be controlled by silicon wafer heating temperature and cooling rate, etc. treatment conditions.

Operation of the Invention

For the silicon wafer having undergone heat treatment according to this invention, non-uniformly distributed internal defect growth nuclei introduced during silicon single crystal growth mostly disappear, and atomic vacancies are newly distributed uniformly at high concentration. Therefore internal defects are generated with a uniform distribution in the silicon wafer during device manufacturing processes. Also the device active region in the vicinity of the surface has a reduced interstitial oxygen concentration so that there is no internal defect generation whatsoever, thereby forming a so-called defect-free zone (DZ).

Results of the Invention

The present invention, due to performance of high temperature heating and rapid cooling of a silicon wafer grown by the CZ method before use of the silicon wafer in device manufacturing processes, can cause internal defect formation that is uniform within the silicon wafer and across the silicon wafer surface and can cause improvement of device characteristics.

Working Examples

Working Example 1

As shown in FIG. 1, a silicon wafer 3 was carried upon a support 2 provided within a quartz vessel 1 containing a N_2 gas atmosphere. A halogen lamp 5 equipped with a light-concentrating mirror 4 was provided above the vessel as a lamp heating apparatus. This invention was carried out under the following conditions.

Silicon wafer

A B-doped silicon single crystal ingot adjusted to have a specific resistivity of 10 Ω-cm was processed into wafers by the conventional method.

Heating method

5 minutes of heating at 1300°C.

Cooling method

Atmospheric cooling.

A comparison wafer was used consisting of the untreated silicon wafer. The above mentioned working example and the comparison wafer were sampled. After thermal oxidation of the samples at 1000°C, and then 5 minutes of treatment with a selective etching solution (Wright solution), internal defects were examined. These results are shown in FIG. 2. FIG. A of this figure is the silicon wafer produced according to this invention. This had no internal defects in the vicinity of the surface. The only internal defects were generated uniformly within the wafer. Mean concentration of these internal defects was 10^5 cm^{-2}. However, FIG. B is the silicon wafer having undergone conventional heat treatment. Internal defects were generated at high density at the outer perimeter of the wafer. These internal defects were non-uniformly distributed throughout the entire volume at a mean density of 10^4 cm^{-2}.

Working Example 2

A silicon wafer was used that was the same as that of working example 1, and MOS memory elements were produced. Then leakage testing was carried out using samples taken from within this silicon wafer. These results are shown in FIG. 3. The plotted solid line indicates the working example of this invention. The plotted dashed line indicates the conventional example. The wafer produced by this invention (solid line) had a leakage failure rate that was uniform across the surface. In contrast, the conventional wafer (dashed line) was found to have a high leakage failure rate in the perimeter region and a non-uniform surface distribution. Moreover, leakage failure rate was found to be lower overall for the wafer of the present invention in comparison to the conventional wafer.

4. Simple Explanation of the Figures

FIG. 1 is an explanatory drawing showing an example of a silicon wafer heating apparatus for carrying out this invention. FIG. 2 shows internal defects of a silicon wafer, wherein FIG. A was produced as a working example of the present invention, and FIG. B is a conventional non-treated wafer. FIG. 3 is a graph showing leakage test results for a working example.

1	....	quartz vessel
2	....	support
3	....	silicon wafer
4	....	mirror
5	....	halogen lamp

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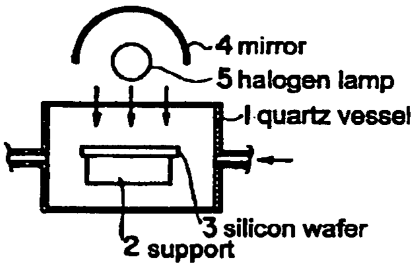
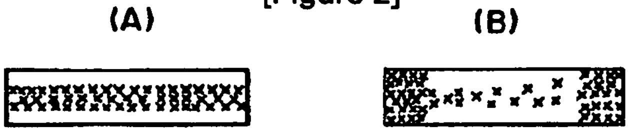
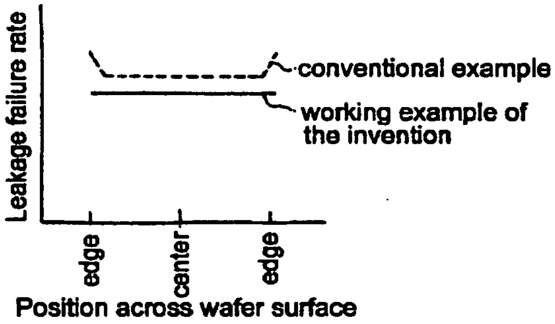
[Figure 1]



[Figure 2]



[Figure 3]



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Claim:

A method for producing a silicon wafer for a semiconductor device comprising the steps of:

heating a silicon wafer for a semiconductor device with a xenon lamp or halogen lamp to a temperature of 1200°C or higher and

then quenching said wafer to a room temperature at a cooling rate of at least 2.2°C/sec.

Page 2, Upper right column, lines 14-16

The heating with the lamp is preferably carried out in an atmosphere of an inert gas such as high purity nitrogen.

Page 2, Lower left column, lines 3-11

In the silicon wafer which is heat-treated according to the present invention, the heterogeneous nuclei generating internal defects, which are introduced during the growth of the silicon single crystal, substantially disappear, and uniform internal defects are formed in the silicon wafer with the atomic vacancies, which are uniformly distributed at a high concentration, in the course of the production of a device. In the device active region near the surface, no internal defects are formed since the concentration of the interstitial oxygen decreases, and thus a so-called defect zero (DZ) layer is formed.

Example 1

As shown in Fig. 1, a silicon wafer (3) was placed on a support (2) which was provided in a quartz vessel (1) containing N2 gas as an atmospheric gas. Using a heating device having a halogen lamp (5) equipped with a converging mirror (4), the wafer was heated according to the present invention under the following conditions:

Silicon wafer:

A silicon wafer fabricated from a rod of a silicon single crystal the resistivity of which is adjusted to 10Ωcm with B-doping.

Heating conditions:

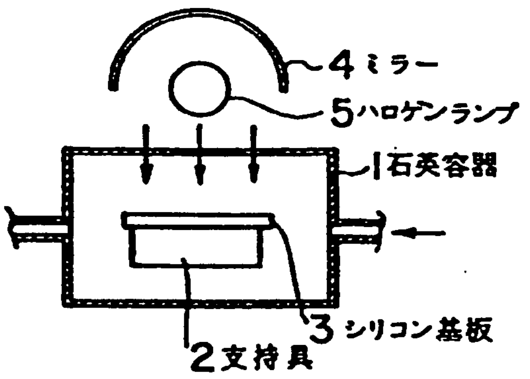
5 minutes at 1300°C

Cooling conditions:

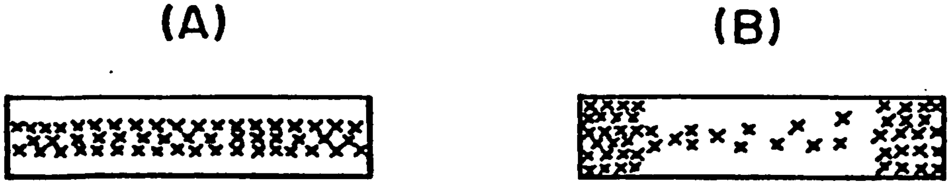
Cooling in an air

The sample of the above-treated wafer and also a comparative sample, which was collected from the silicon wafer as such and heated at 1000°C for 16 hours, were treated with a selective etching liquid (Wright reagent) for 5 minutes to inspect the internal defects. The results are shown in Fig. 2. Fig. 2(A) is for the wafer of the present invention. There was no defects near the surfaces, and the defects were uniformly generated in the inside of the wafer. The average concentration of the defects was $10^5/cm^2$. Fig. 2(B) is for the wafer which was not treated according to the present invention. The internal defects were heterogeneously generated near the periphery of the wafer at a high concentration. The average concentration of the defects was $10^4/cm^2$.

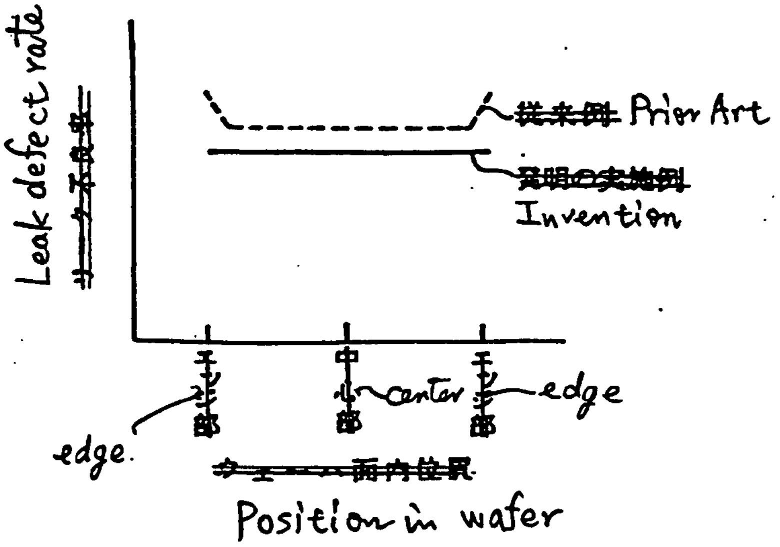
~~第1図~~ Fig.1



~~第2図~~ Fig.2



~~第3図~~ Fig.3



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審査請求　未請求　請求項の数　1　（全３頁）

㉔発明の名称　半導体デバイス用シリコン基板の製造方法

㉑特　　願　昭63－182668

㉒出　　願　昭63(1988) ７月21日

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明　細　書

１．発明の名称

半導体デバイス用シリコン基板の製造方法

２．特許請求の範囲

１　半導体デバイス用シリコン基板にキセノンランプ又はハロゲンランプによる光を照射して1200℃以上に加熱した後、常温まで 2.2℃／sec 以上の速度で急冷することを特徴とする半導体デバイス用シリコン基板の製造方法。

３．発明の詳細な説明

産業上の利用分野

この発明は、半導体デバイス用シリコン基板の製造方法に関する。

従来の技術

半導体デバイスに用いられるシリコン基板は、ほとんどが引上げ法（ＣＺ法）で育成されたものである。

このＣＺ法で育成されるシリコン単結晶には、通常10^{18} 個/㏄程度の酸素不純物が含まれており、そのままの状態でデバイス製造工程に使用すると、工程中に過飽和な酸素不純物が析出する。又、この酸素析出物の体積膨張による歪みで二次的に転位、積層欠陥等が発生する（以下、これら析出物、転位、積層欠陥等を単に内部欠陥と称す）。

これらの内部欠陥は、半導体デバイスの特性に大きな影響を及ぼす。デバイス活性層に欠陥がある場合、リーク電流の増大、酸化膜耐圧不良等を引き起す。一方、デバイス製造工程で導入される汚染不純物のゲッタリング源となり、デバイス特性が向上する。したがって、内部欠陥の発生を制御することが重要である。

従来、ＣＺ法により育成されたシリコン単結晶はウエハに加工されてシリコン基板として、そのままデバイス製造工程に使用されている。

発明が解決しようとする課題

前記のごとく、ＣＺ法で育成されたシリコン基板はそのままデバイス製造工程に使用すると、シリコン単結晶育成時に受ける熱履歴により導入された発生核に応じた分布で内部欠陥が発生する。その結果、内部欠陥は基板内で不均一に発生し、

デバイス特性を悪化させていた。

この発明は、前記問題点を解消するための方法を提供することを目的とする。

課題を解決するための手段

この発明は、半導体デバイス用シリコン基板にキセノンランプ又はハロゲンランプによる光を照射して1200℃以上に加熱した後、常温まで 2.2℃/sec 以上の速度で急冷することにある。

この発明は、シリコン基板をデバイス製造工程以前において、前記のごとく熱処理を施すことにより、デバイス製造工程でシリコン基板間及びシリコン基板面内均一に内部欠陥を形成する性質を付与することにある。

前記熱処理により、シリコン基板の格子間酸素が外方拡散し表面近傍の格子間酸素濃度が減少する。又、シリコン単結晶育成時に導入される内部欠陥の発生核は温度に依存する臨界サイズにより、その成長、消滅が左右されるため、当該シリコン基板の内部欠陥発生核は、そのほとんどが縮少、消滅する。加えて、格子間シリコン原子は拡散によりその濃度が減少し、当該シリコン基板は原子空孔濃度が高くなる。

前記熱処理における加熱温度は、1200℃未満では格子間酸素の外方拡散及び内部欠陥発生核の消滅に要する時間が長くなる。

又、加熱後は外気に触れる等の手段により常温まで急冷するが、この急冷処理により冷却中における新たな内部欠陥の発生核の導入が抑制される。さらに高濃度の原子空孔は当該シリコン基板内に均一に分布した状態で凍結される。

又、加熱方法としてキセノンランプ又はハロゲンランプを使用するのは、拡散炉に比べより高温に加熱することができ、さらに昇温速度が大きく加熱時間を短縮できるためである。なお、この光ランプによる加熱は高純度窒素ガス等の不活性ガス雰囲気で行うことが望ましい。その理由は、格子間酸素の外方拡散を増し、又加熱中の雰囲気による汚染を少なくすることにある。

なお、内部欠陥の発生密度はシリコン基板の加熱温度及び急冷速度等の処理条件により制御することができる。

作　用

この発明の実施により熱処理されたシリコン基板は、シリコン単結晶育成時に導入された不均一な内部欠陥発生核は、そのほとんどが消滅し、新たな高濃度の均一に分布する原子空孔により、シリコン基板はデバイス製造工程中均一に内部欠陥が発生する。そして、表面近傍のデバイス活性領域は、格子間酸素濃度が減少しているため内部欠陥の発生は皆無となり、いわゆる無欠陥領域（ＤＺ層）が形成される。

発明の効果

この発明は、ＣＺ法で育成されたシリコン基板を、デバイス製造工程で使用する前に、高温加熱－急冷の熱処理を施すことにより、デバイス製造工程においてシリコン基板間及びシリコン基板面内均一に内部欠陥を形成する性質を付与することができ、デバイス特性の向上に寄与できる。

実　施　例

実施例１

第１図に示すように、N_2 ガスを雰囲気ガスとする石英容器(1)内に設けた支持具(2)にシリコン基板(3)を載せ、容器上方には集光用のミラー(4)を有するハロゲンランプ(5)を設けてなる光ランプ加熱装置を使って、次の条件でこの発明を実施した。

シリコン基板

Ｂドープにより比抵抗10Ωcmとなるように調整したシリコン単結晶棒を通常の方法でウエハ加工したもの。

加熱方法

1300℃で 5 min加熱

冷却方法

大気中冷却

前記実施例による試料と共に比較のため、前記シリコン基板のままの試料を採り1000℃で16hr熱酸化後、選択エッチング液（ライト液）で 5分間処理して内部欠陥を調べた。その結果を第２図に示す。そのＡ図はこの発明の実施によるシリコン基板であり、内部欠陥は表面近傍には皆無であり、内部のみに均一に発生し、その平均密度は10^5

個/㎠であった。一方B図は従来の熱処理を施さない場合のシリコン基板であり、内部欠陥は基板外周に高密度で発生しており、その平均密度は10^4個/㎠で全体に不均一に発生していた。

実施例２

実施例１におけるシリコン基板と同じものを使って、MOS メモリー素子を作製した。そして、それらの中から採った試料についてリーク試験を行った。その結果を第３図に示す。実線はこの発明の実施例によるもの、破線は従来のものであり、この発明によるもの（実線）はリーク不良率が面内均一であるに対し、従来のもの（破線）は面内不均一で外周部のリーク不良率が高いことがわかる。又、全体的に見てこの発明によるものは従来のものに比べてリーク不良率が低いことがわかる。

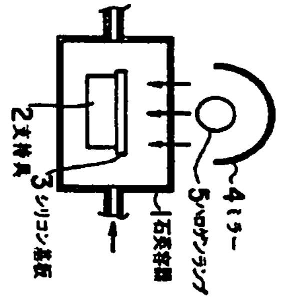
４．図面の簡単な説明

第１図はこの発明を実施するためのシリコン基板加熱装置の一例を示す説明図、第２図はシリコン基板の内部欠陥を示す図面で、A図はこの発明の実施例によるもの、B図は従来の非処理のもの、第３図は実施例におけるリーク試験結果を示すグラフである。

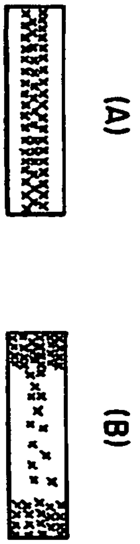
1…石英容器	2…支持具
3…シリコン基板	4…ミラー
5…ハロゲンランプ	

出願人　九州電子金属株式会社
同　大阪チタニウム製造株式会社
代理人　弁理士　押田良久

第１図



第２図



第３図